CptS 260 Final Exam Study Guide

Fall, 2021

The final will be two hours long. Closed everything, except for a copy of the MIPS "green card" and you may use a "Jot" (or similar) calculator. No cellphones, tables, laptops, or other electronics are permitted.

1. Introduction (Chapter 1)
2. Machine Instructions (Chapter 6)
    - instruction set architecture
    - registers
    - address ranges
    - assembler implementation of higher-level concepts (e.g. linked lists)
3. Computer Arithmetic (Chapters 1 and 5)
    - powers of two
    - signed and unsigned arithmetic
    - floating point computation
4. Digital Logic and Digital Systems (Chapters 1, 2, and 3)
    - Boolean logic circuits
    - latches
    - flip-flops
    - Karnaugh maps

    (midterm)
5. Processor Architecture (Chapters 5, 6, and 7)
    - architecture vs. microarchitecture
    - mapping instruction fields to control and data signals
    - processor stages
    - processor block diagrams
    - data and control flow for instructions
        - cycle time determination
    - single-cycle vs. multicycle vs. pipelined
    - multiplexers
    - decoders
    - pipelining
        - benefits
        - architectural demands made by pipelining
        - stall causes and avoidance

6. Memory System Organization and Architecture (Chapters 3, 5, and 8)
    - the memory hierarchy
        - typical access times
    - memory types
    - caching
        - address partitioning
        - cache mapping
            - direct
            - N-way associative
            - fully associative
        - spatial and temporal locality
        - hit/miss computation
        - cache miss types and strategies
            - compulsory
            - capacity
            - conflict
7. Interfacing and Communication (Chapter 8)
    - memory mapped I/O
        - address decoder
8. Multiprocessing (Chapter 7)
    - need for parallel processing
    - Amdahl's Law
    - parallelism
        - multiple-issue architectures
        - speculation
        - very long instruction words (VLIW)
            - scheduling left up to compiler
        - superscalar
            - hardware organizes parallel use
    - multicore
    - multithreading
9. Cybersecurity
    - (not on the final)
10. Alternative Architectures
    - design choices (e.g. instruction lengths)

- RISC vs. CISC