Project (optional) **Due: 5:00pm, 12/17 (no late turn-ins)**

This project is optional. Students who successfully complete it will earn 10 points of extra credit, which will be added to their grades after all other grade computations and letter grade mappings have been made. If you choose not to attempt it, your grade will not be affected.

Grading will be very strict. Partial credit will probably be rare.

The due date listed above is firm. No late turn-ins will be permitted.

Numerical grades will be assigned as usual, but no evaluation will be provided.

The MIPS++ Architecture

Suppose you work for a company that is looking to design an architecture called "MIPS++" that is upwardly compatible with the 32-bit MIPS architecture. Marketing has decided that in order to compete with the MIPS, the MIPS++ must support 64 32-bit registers while the MIPS has 32.

An architecture consists of a description of the instruction set, registers, and memory layout. The number (64) and size (32 bits) of the registers are given and the memory layout is the same, so it's up to you to fill in the details of the instruction set architecture.

For compatibility with existing compilers, the MIPS++ assembler will accept the same mnemonics (`add`, `lw`, `jal`, etc.) but the instruction formats may have to change in order to support the functionality of the original MIPS.

Your assignment is to provide a 1-2 page written report describing the MIPS++ instruction set architecture and any necessary changes to the three microarchitectures we've described in class. Effectively, this will describe changes needed for the MIPS++ "Green Card".

This is a "real" report. The writing should be clear. Check grammar and spelling. Be as quantitiative as possible. Diagrams are encouraged.